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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/571,142	11/22/2006	Kenshi Fukumitsu	46884-5461	3680

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EXAMINER	
WHALEN, DANIEL B	
ART UNIT	PAPER NUMBER
2829	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/571,142	FUKUMITSU ET AL.	
	Examiner	Art Unit	
	DANIEL WHALEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/312007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/22/2006 and 07/31/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: in lines 17-19, "a plurality of semiconductor chips each having a front face formed… in close contact with a rear face thereof" should be read --a plurality of semiconductor chips each having the front face formed…in close contact with the rear face thereof-- in order to correct antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami (US 2003/0190795 A1) in view of Sawada (US 2002/0115235 A1) and Kurosawa et al. (US 6,756,562 B1; hereinafter "Kurosawa").

Regarding Claim 9, Kawakami teaches a semiconductor substrate cutting method for cutting a semiconductor substrate having a front face formed with a plurality of functional devices into the individual functional devices, so as to manufacture a semiconductor device having the functional device, the method comprising the steps of:

attaching a protective member (15) to the front face (main surface) of the semiconductor substrate (2), such that the functional devices (semiconductor chips 3) are covered (fig. 3);

singulating the semiconductor substrate into individual functional devices (fig. 5);

mounting the semiconductor chip onto a support body (2a), so as to obtain the semiconductor device (fig. 7).

However, Kawakami does not explicitly disclose attaching an expandable holding member to the rear face of the semiconductor substrate by way of a die bonding resin layer; and mounting the semiconductor chip onto a support body by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor device. Sawada discloses attaching an expandable holding member (S) to the rear face of the semiconductor substrate by way of a die bonding resin layer (AD); cutting the semiconductor substrate and the die bonding resin layer, so as to obtain a plurality of semiconductor chips (P) each having a cut piece of the die bonding resin layer in close contact with the rear face thereof (fig. 13B); and mounting the semiconductor chip onto a support body (R) by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor device (fig. 13D) (paragraph 12-13). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the teaching of Kawakami with that of Sawada so as to reduce time of the fabrication process with improved reliability.

However, the combined teaching of Kawakami and Sawada does not explicitly disclose that singulating the semiconductor substrate is performed by laser light. Kurosawa disclose that singulating process is performing by irradiating the semiconductor substrate with laser light (29) while positioning a light-converging point within the semiconductor substrate (fig. 17) with a rear face (21B) of the semiconductor substrate acting as a laser light incident face after the step of attaching the protective member (22), so as to form a modified region (30-1,30-2,30-3), and causing the modified region to form a starting point region for cutting along each line along which the semiconductor substrate should be cut (col. 7, lines 15-19a), the lines set like a grid running between the neighboring functional devices, inside by a predetermined distance from the laser light incident face (fig. 16-18); cutting the semiconductor substrate and the die bonding resin layer from the starting point regions for cutting along each of the lines in the grid by expanding the holding member after attaching the holding member, so as to obtain a plurality of semiconductor chips each having a front face formed with the functional device (fig. 25) (col. 2, lines 17-29). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the teaching of Kawakami and Sawada with that of Kurosawa so as to effectively singulate the semiconductor substrate into individual functional devices without cutting streaks such as scratches or distortions on the side surface of the individual functional devices.

It is noted that when the light positions to the rear face of the semiconductor substrate, the rear face acts at a laser light incident face.

Regarding Claim 10, Kurosawa teaches that wherein the support body is a lead frame (2a).

4. **Claims 9 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno et al. (US 2003/0077879 A1; hereinafter "Ohno") in view of Sawada and Fukuyo et al. (US 2004/0002199 A1; hereinafter "Fukuyo")

5. **Regarding Claim 9**, Ohno teaches a semiconductor substrate cutting method for cutting a semiconductor substrate having a front face formed with a plurality of functional devices into the individual functional devices, so as to manufacture a semiconductor device having the functional device, the method comprising the steps of:

attaching a protective member (18) to the front face (12) of the semiconductor substrate (10), such that the functional devices are covered (fig. 9A);

singulating the semiconductor substrate into individual functional devices (fig. 9E);

mounting the semiconductor chip (16) onto a support body (32) so as to obtain the semiconductor device (fig. 9F).

However, Ohno does not explicitly disclose attaching an expandable holding member to the rear face of the semiconductor substrate by way of a die bonding resin layer; and mounting the semiconductor chip onto a support body by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor device. Sawada discloses attaching an expandable holding member

(S) to the rear face of the semiconductor substrate by way of a die bonding resin layer (AD); cutting the semiconductor substrate and the die bonding resin layer, so as to obtain a plurality of semiconductor chips (P) each having a cut piece of the die bonding resin layer in close contact with the rear face thereof (fig. 13B); and mounting the semiconductor chip onto a support body (R) by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor device (fig. 13D) (paragraph 12-13). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the teaching of Ohno with that of Sawada so as to reduce time of the fabrication process with improved reliability.

However, the combined teaching of Kawakami and Sawada does not explicitly disclose that singulating the semiconductor substrate is performed by laser light. Fukuyo discloses irradiating the semiconductor substrate with laser light (L) while positioning a light-converging point (P) within the semiconductor substrate (1), so as to form a modified region (9), and causing the modified region to form a starting point region for cutting along each line along which the semiconductor substrate should be cut, the lines set like a grid running between the neighboring functional devices, inside by a predetermined distance from the laser light incident face (fig. 102; paragraph 527-528); and cutting the semiconductor substrate from the starting point regions for cutting along each of the lines in the grid by expanding the holding member after attaching the holding member, so as to obtain a plurality of semiconductor chips each having a front face formed with the functional device (fig. 107; paragraph 117, 562-563). Therefore, it

would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the teaching of Kawakami and Sawada with that of Kurosawa so as to singulate the semiconductor substrate without generating melt or unnecessary fractures deviating from the line along which the semiconductor substrate is intended to be cut.

It is noted that it would have been obvious to one of the ordinary skill in the art would recognize that the light can be emitted either the front face of the rear face of the semiconductor substrate so as to form the modified region within the substrate as it is a readily available method. Furthermore, when the laser light is emitted to the surface, the surface acts at a laser light incident face.

Regarding Claim 11, Ohno teaches that wherein the holding member is expanded (cutting step) after the protective member is removed from the front face of the semiconductor substrate (fig. 9D-9E).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WHALEN whose telephone number is (571)270-3418. The examiner can normally be reached on Monday-Friday, 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2829
07/15/2008

Daniel Whalen
/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829